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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,891	11/21/2003	George P. Hoekstra	SC12730TC	1652

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,891	HOEKSTRA, GEORGE P.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/21/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9, 15, 16, 19-24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Levy et al. (US 5,825,208).

3. With respect to claims 1 and 17, figure 5 of Levy teaches a multistage dynamic domino circuit comprising:

a footed dynamic domino stage (stage 1) including:

a first precharge circuit (502);

evaluation logic (504); and

a data output (515) coupled to the evaluation logic;

a footless dynamic domino stage (stage 2) including:

evaluation logic (516) including a data input coupled to the data output of the footed dynamic domino stage; and

a second precharge circuit including:

a first precharge device (514) including a first current terminal and a control terminal coupled to a clock line (530); and

a second precharge device (512) including a first current terminal coupled to the first current terminal of first precharge device and a control terminal; and

a delay circuit (526) including an input coupled to the clock line and an output coupled to the control terminal of the second precharge device to provide a delayed version of a clock signal provided at the input of the delay circuit.

4. With respect to claim 2, figure 5 of Levy teaches the first precharge circuit includes a P-channel device (502) having control terminal coupled to the clock line.

5. With respect to claim 3, figure 3A of Levy teaches the delay circuit includes:

a first inverter including an input coupled to the input of the delay circuit and an output; and

a second input including an input coupled to the output of the first inverter and the output coupled to the output of the delay circuit.

6. With respect to claim 4, figure 6 of Levy discloses the footed dynamic domino delay stage has a falling edge delay from a precharge edge of a clock signal provided to the precharge circuit of the footed dynamic domino stage to a falling edge of the data output; and

the delay circuit providing the delayed version with a delay of greater than the falling edge delay.

7. With respect to claim 5, figure 5 of Levy discloses the first precharge circuit (514) is coupled to the clock line, wherein the clock signal is provided to the first precharge circuit via the clock line.

8. With respect to claim 6, figure 5 of Levy teaches the control terminal of the first precharge device is connected to the clock line;

the input of the delay circuit is connected to the clock line; and

the output of the delay circuit is connected to the control terminal of the second

precharge device (512).

9. With respect to claim 7, figure 5 of Levy discloses the first precharge circuit of the footed dynamic domino circuit includes a third precharge device (508) including a control terminal, the control terminal of the third precharge device is connected to the clock line.

10. With respect to claim 8, figure 6 of Levy discloses during a precharge phase following an evaluation phase, the output of the delay circuit falls after a falling edge of the data output occurring during the precharge phase.

11. With respect to claim 9, figure 6 of Levy discloses wherein entering an evaluation phase, the control terminal of the first precharge device receives a rising edge prior to a rising edge of the data out during the evaluation phase.

12. With respect to claim 15, the apparatus of Levy is designed with integrated circuit.

13. With respect to claim 16, figure 5 of Levy discloses the first precharge device is a P-channel device (514); the second precharge device is a second p-channel device (512).

14. With respect to claims 19-24, the methods therein are inherent given the apparatus of Levy as shown in the above rejections.

15. With respect to claim 25, figure 5 of Levy discloses a multistage dynamic domino circuit comprising:

a footed dynamic domino stage including:

a first precharge circuit including a P-channel device (502), the P-channel device including a control terminal coupled to a clock line;

evaluation logic including at least one N-channel device (504); and

a data output coupled to the evaluation logic;

a footless dynamic domino stage including:

evaluation logic (516) including a data input coupled to the data output of the footed dynamic domino stage, the evaluation logic including at least one N- channel device; and

a second precharge circuit including:

a second P-channel device (514) including a first current terminal and a control terminal coupled to the clock line; and

a third P-channel device (512) having a first current terminal coupled to the first current terminal of second P-channel device and a control terminal; and

a delay circuit (526) including an input coupled to the clock line and an output coupled to the control terminal of the third P-channel device to provide a delayed version of a clock signal provided on the clock line.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 10-14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy al. (US 5,825,208).

18. With respect to claims 10-14, for simplicity, Levy shows only three stages in the disclosure. However, Levy stated that the design can have multiple stages of identical circuits (see column 4, lines 60-65). It would have been obvious to one of ordinary skill of art at the time

the invention was made to have multiple identical stages as taught by Levy and as a design choice.

19. With respect to claim 18, Levy does not specifically disclose a processor as claimed by applicant. However, it is notoriously well known in the art that logic circuitry is used with processor to form a complex circuits. It would have been obvious to one of ordinary skill of art at the time the invention was made to have used the logic circuitry of Levy with other electrical circuit such as processor for the purpose of designing a complex electrical circuit.

120. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/28/2005

DON LE
PRIMARY EXAMINER